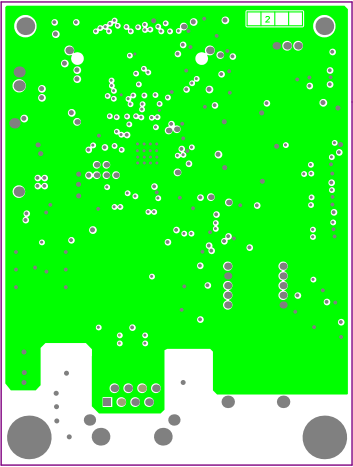
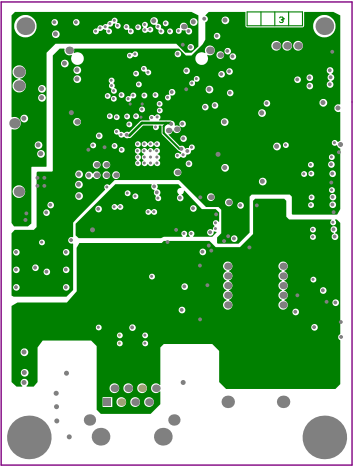


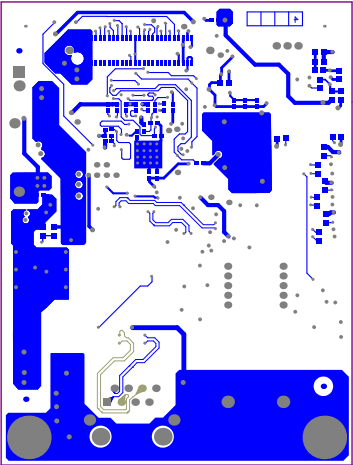
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #:	TI DA-00496-CU	REV:	E1	SUN REV:	Not In VersionControl
LAYER NAME =	Top Layer					
PLOT NAME =	Top Layer	GENERATED :	9/23/2015	5:39:12 AM	TEXAS INSTRUMENTS	



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00496_CU	REV: E1	SUN REV: Not In VersionControl
LAYER NAME = L2_P1			
PLOT NAME = L2_P1	GENERATED : 9/23/2015 9:39:12 AM	TEXAS INSTRUMENTS	



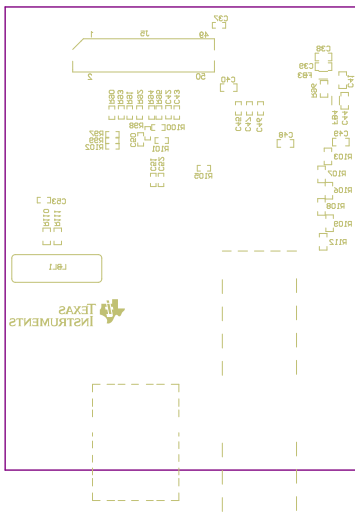
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #:	TIDA-00496_CU	REV:	E1	SUN REV:	Not In VersionControl
LAYER NAME =	L3_P2					
PLOT NAME =	L3_P2	GENERATED :	9/23/2015	5:39:12 AM	TEXAS INSTRUMENTS	



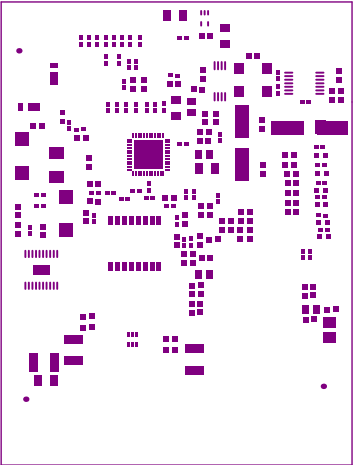
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LAYER NAME =	Bottom Layer					
PLOT NAME =	Bottom Layer	GENERATED :	9/23/2015	5:39:13 AM	TEXAS INSTRUMENTS	



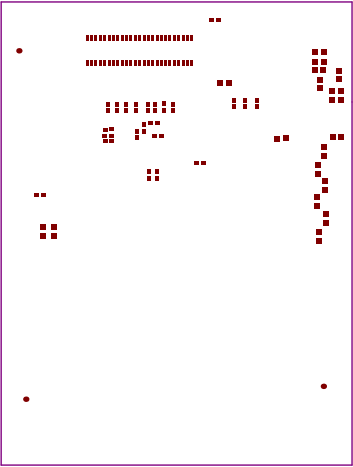
TEXAS INSTRUMENTS



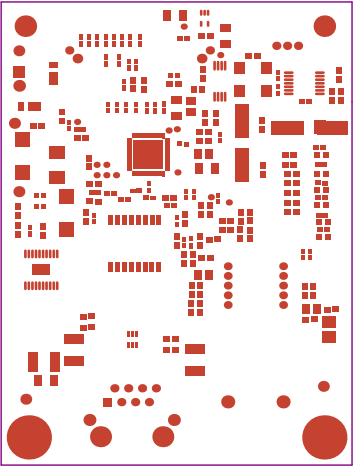
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LAYER NAME = Bottom Overlay			
PLOT NAME = Bottom Silkscreen Overlay	GENERATED : 9/23/2015 9:55:13 AM		TEXAS INSTRUMENTS



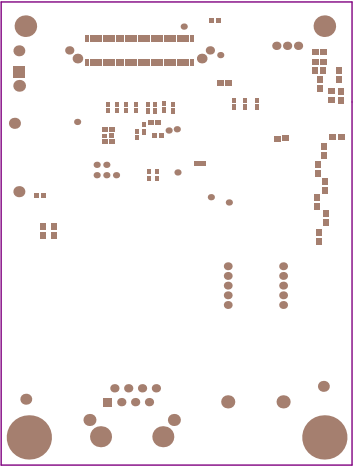
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00496_CU	REV: E1	SUN REV: Not In VersionControl
LAYER NAME = Top Paste			
PLOT NAME = Top Paste Mask Print	GENERATED : 9/23/2015 9:39:13 AM	TEXAS INSTRUMENTS	



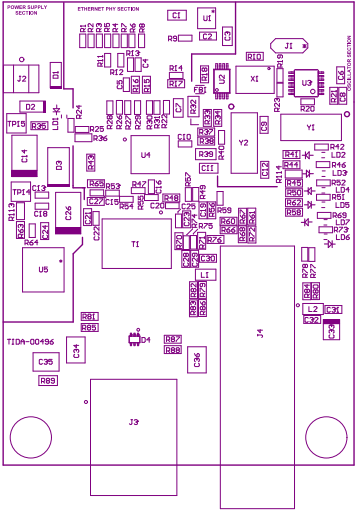
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00496_CU	REV: E1	SUN REV: Not In VersionControl
LAYER NAME = Bottom Paste			
PLOT NAME = Bottom Paste Mask Print	GENERATED : 9/23/2015 9:39:13 AM	TEXAS INSTRUMENTS	



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00496_CU	REV: E1	SUN REV: Not In VersionControl
LAYER NAME = Top Solder Mask			
PLOT NAME = Top Solder Mask Print	GENERATED : 9/23/2015 9:39:14 AM	TEXAS INSTRUMENTS	



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #:	TIDA-00496_CU	REV:	E1	SUN REV:	Not In VersionControl
LAYER NAME =	Bottom Solder Mask					
PLOT NAME =	Bottom Solder Mask Print	GENERATED :	9/23/2015	9:39:14 AM	TEXAS INSTRUMENTS	



ASSEMBLY VARIANT:
COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
[No Variations]

PCB VIEWED FROM TOP SIDE		BOMID #: TIDN-00496_CU	REV: EI	SUN REV: Not In VersionControl
LAYER NAME : Assembly TOP				
PLOT NAME = /P5 Assembly Top		GENERATED : 8/23/2015 9:39:14 AM		TEXAS INSTRUMENTS

Layer Stack Up Detail for: TIDA-00496_CU.PcbDoc			
Layer Name	Layer Description	Copper Thickness	Dielectric Material
Top Solder Mask	<.6TS>		Solder Resist
Top Layer	<.6TL>	1.4mil	FR-408
L2_P1	<.6B1>	1.4mil	FR-408
L3_P2	<.6B2>	1.4mil	FR-408
Bottom Layer	<.6BL>	1.4mil	FR-408
Bottom Solder Mask	<.6BS>		Solder Resist

DESIGN INFORMATION

BOARD SIZE (REFER ALSO ARRAY/PANEL PROFILING INFORMATION)
2535.00mi X 3346.46mi

Number of Layers : 4
MIN. TRACK WIDTH: 7 MIL
MIN. CLEARANCE: 7.8 MIL
MIN. VIA PAD SIZE: 26 MIL

MINIMUM ANNUAL RING 0.177mm (7MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- .5 MIL, HOLES +/- .3 MIL
IT IS IMPEDANCE CONTROLLED BOARD

MATERIAL:
☒ FR-408 ☐ FR-4 High Tg ☐ OTHER _____

THICKNESS: ☒ 63 MIL (1.6mm) +/-10% ☐ OTHER _____

TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____

BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____

COPPER THICKNESS (FINISHED):
OUTER: ☒ 1.4MIL (1oz) ☐ 2MIL (1.4oz) ☐ 2.8MIL (2oz)
INNER SIGNAL: ☒ 1.4MIL (1oz) ☐ 2.8MIL (2oz) ☐ N/A

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH MIN COPPER THICKNESS: ☒ 1MIL ☐ OTHER _____

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER _____
SOLDER RESIST COLOR:
☒ GREEN ☐ BLUE ☐ OTHER _____

SURFACE FINISH: ☒ IMMERSION GOLD (ENG) ☐ ENERPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER _____

ARRAY/PANEL: ☐ CUT AND TRIM PER MECH LAYER 1
☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ UL 94V-0 ☒ RoHS ☐ OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES VIA TENTING: ☐ NONE ☒ REQUIRED
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
MANUFACTURER'S UL: ☐ RAIL ☐ METAL ☒ SILK



PROJECT TITLE: IEEE1588 ethernet Brick-Copper	
DESIGNED FOR: Public Release	
FILE NAME: TIDA-00496_CU.PcbDoc	
ENGINEER: Srinivas Kalikuppa	LAYOUT BY: Anuradha
SCALE: 1:00	
ALTIM DESIGNER VERSION: 14.3.14.34663	

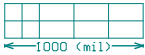
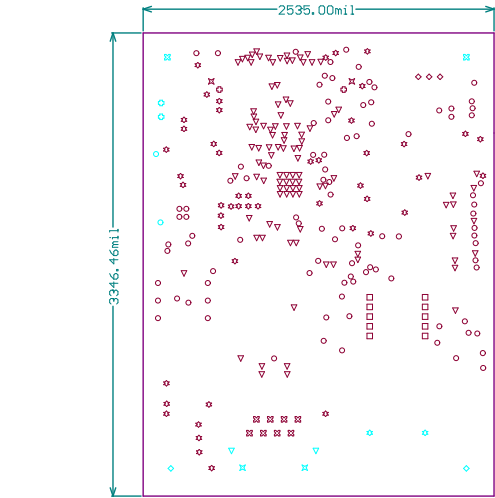
IMPEDANCE TABLE

LAYER	TRACE WIDTH	SPACING	IMPEDANCE	REFERENCE LAYER
TOP	7 MIL	16 MIL	100 OHM +/-10%	L2_P1
BOTTOM	7 MIL	16 MIL	100 OHM +/-10%	L3_P2

Symbol	Hit Count	Tool Size	Plated	Hole Type
▽	107	12mil (0.305mm)	PTH	Round
○	96	16mil (0.406mm)	PTH	Round
●	49	20mil (0.508mm)	PTH	Round
□	10	31.69mil (0.81mm)	PTH	Round
×	3	32mil (0.813mm)	PTH	Round
✕	2	33mil (0.838mm)	PTH	Round
■	8	35.039mil (0.89mm)	PTH	Round
○	2	40mil (1.016mm)	PTH	Round
○	2	44mil (1.118mm)	PTH	Round
○	2	55.119mil (1.4mm)	PTH	Round
○	2	57.087mil (1.45mm)	NPTH	Round
▽	2	62.205mil (1.58mm)	PTH	Round
○	2	125.994mil (3.2mm)	PTH	Round
✕	2	127.993mil (3.25mm)	NPTH	Round
■	2	128mil (3.251mm)	NPTH	Round
291 Total				

Drill Table

DRILL TOLERANCES:
FOR PTH : +/-3MILS
FOR NPTH : +/-2MILS
FOR 12MIL DRILL VIA : +/-12MILS
FOR 16MIL DRILL VIA : +/-16MILS



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00496_CU	REV: E1	SUN REV: Not In VersionControl
LAYER NAME = Drill Drawing			
PLOT NAME = Drill Drawing For (Bottom Layer,Top Layer)	GENERATED : 9/23/2015 9:39:15 AM	TEXAS INSTRUMENTS	

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